

EMLSI SRAM Product Catalog

June 2004

Product List 1

Density	Vcc(Typ.)	Org.	Pkg	Part no.	Remark
1MS	3.3V	x8	32 TSOP 1	EM610FV8T-55/70 LL/LF	
			32 sTSOP 1	EM610FV8S-55/70 LL/LF	
			36 BGA	EM610FV8-55/70 LL/LF	
		x16	44 TSOP 2	EM611FV16U-55/70 LL/LF	
			48 BGA	EM610FV16-55/70 LL/LF	Dual CS
				EM611FV16-55/70 LL/LF	Single CS
2MS	3.3V	x8	32 TSOP 1	EM620FV8AT-55/70 LL/LF	Sample Q3 2004
			32 sTSOP 1	EM620FV8AS-55/70 LL/LF	
			36 BGA	EM620FU8 -55/70 LL/LF	
	3.0V	x16	48 BGA	EM620FU16-55/70 LL/LF	Dual CS
				EM621FU16-55/70 LL/LF	Single CS

55 : 55nsec , 70 : 70nsec

LL : lead , LF : lead free

Product List 2

Density	Vcc(Typ.)	Org.	Pkg	Part no.	Remark			
4MS	3.3V	x8	32 TSOP 1	EM641FV8FT-55/70 LL/LF				
			32 sTSOP 1	EM641FV8FS-55/70 LL/LF				
	3.0V		36 BGA	EM640FU8E-55/70 LL/LF				
	3.3V	x16	44 TSOP 2		EM643FV16FU-55/70 LL/LF	Single CS	tBA=tOE	
					EM644FV16FU-55/70 LL/LF		tBA=tCO	
					EM645FV16FU-55/70 LL/LF	Dual CS	tBA=tOE	
					EM646FV16FU-55/70 LL/LF		tBA=tCO	
	3.0V			48 BGA		EM640FU16E-55/70 LL/LF	Dual CS	
						EM641FU16E-55/70 LL/LF	Single CS	
	1.8V	x8		36 BGA	EM640FP8-70 LL/LF			
			x16		48 BGA	EM640FP16-70 LL/LF	Dual CS	
						EM641FP16-70 LL/LF	Single CS	
	8MS	3.0V	x8	36 BGA	EM680FU8-55/70 LL/LF			
			x16	48 BGA	EM680FU16-55/70 LL/LF	Dual CS		
EM681FU16-55/70 LL/LF					Single CS			

55 : 55nsec , 70 : 70nsec

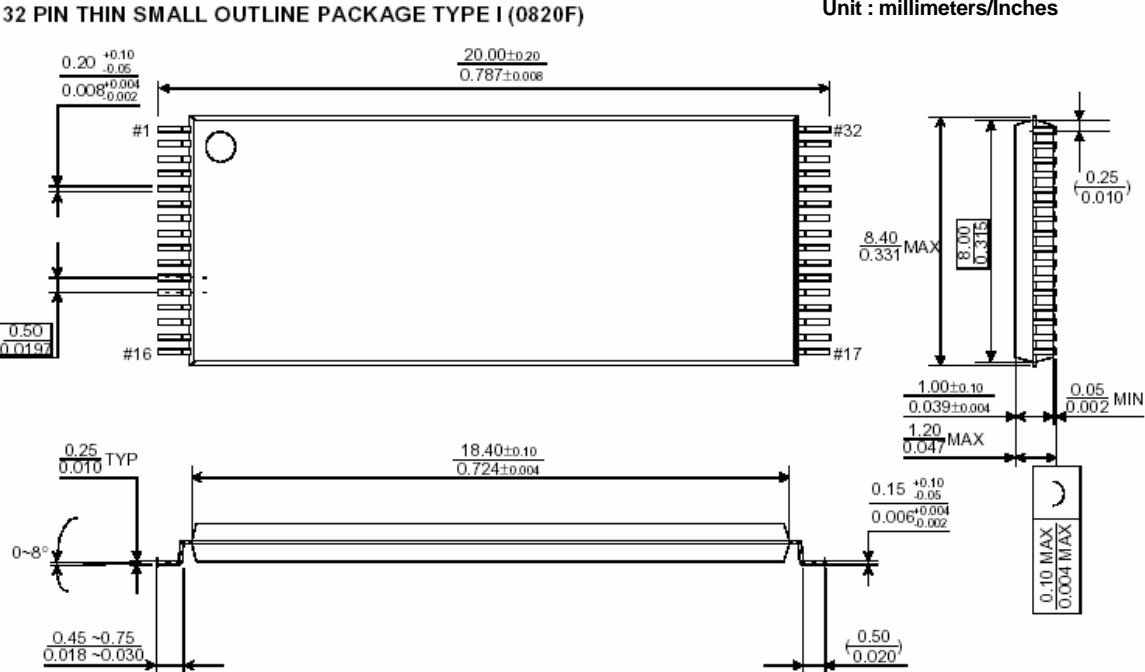
LL : lead , LF : lead free

Confidential Presentation

Emerging Memory & Logic Solutions Inc.(EMLSI)

Package Dimension

32 pin TSOP type I

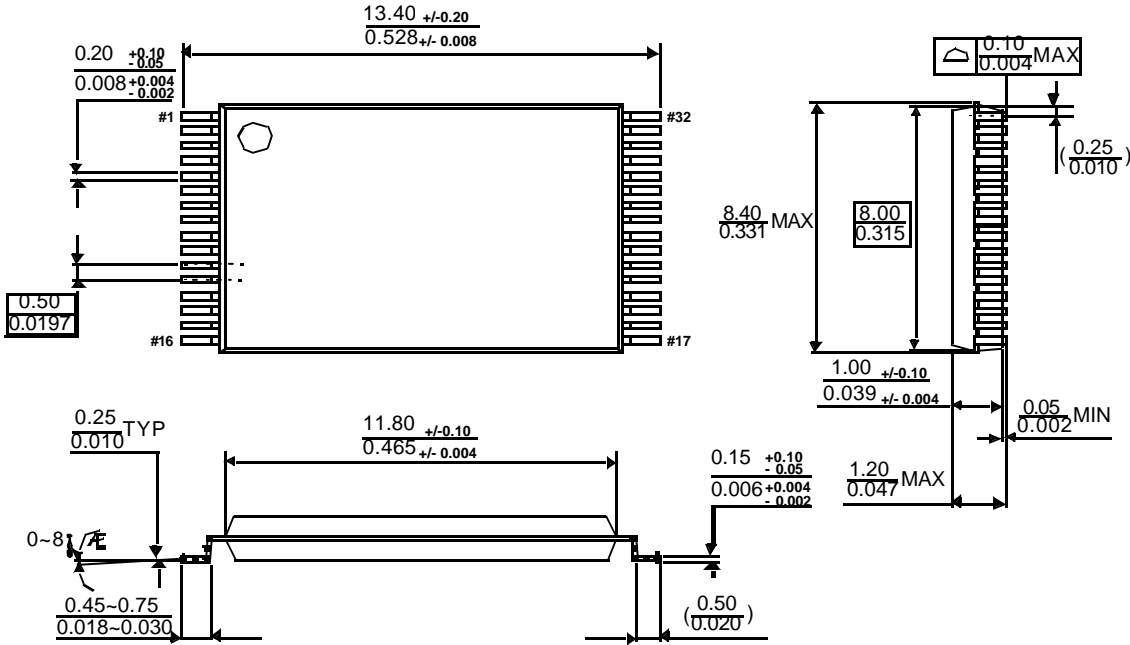


Package Dimension

32 pin sTSP type I

(32-sTSP1-0813.4F)

Unit : millimeters/Inches

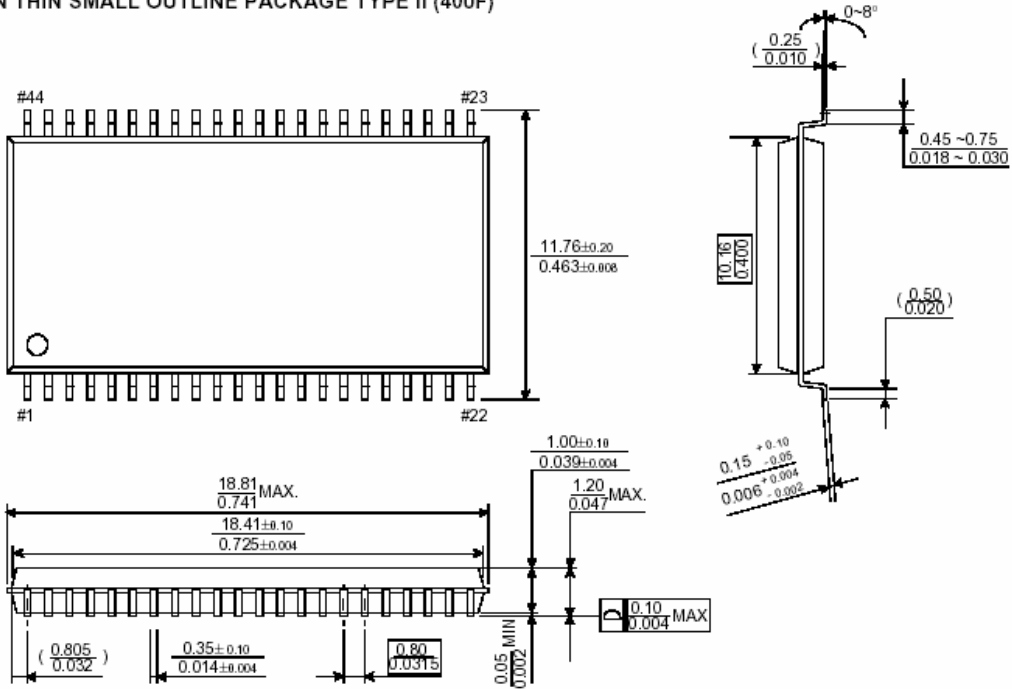


Package Dimension

44 pin TSOP type II

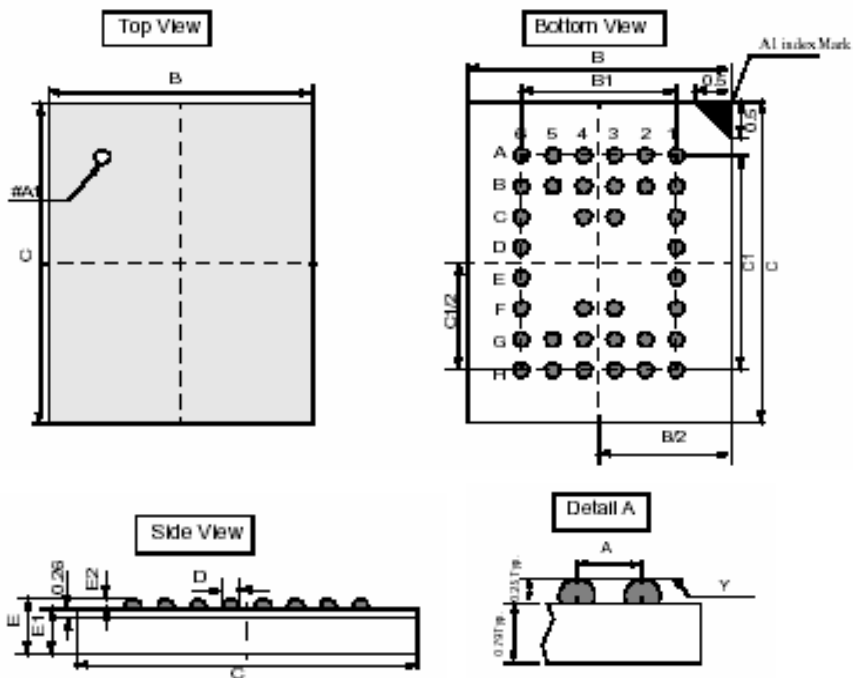
44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)

Unit : millimeters/Inches



Package Dimension

36 pin FpBGA 6 x 7mm



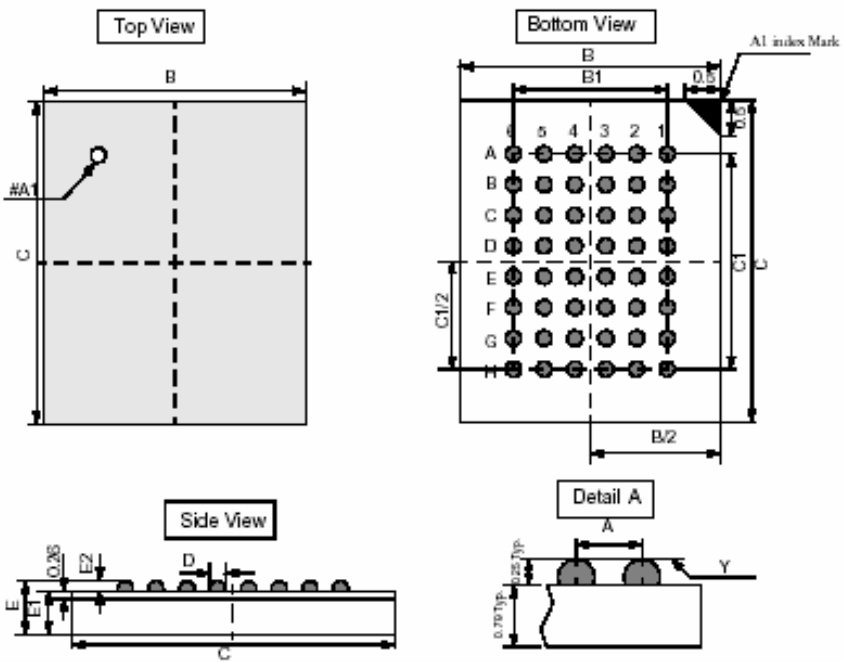
	Min	Typ	Max
A	-	0.75	-
B	5.93	6.00	6.03
B1	-	3.75	-
C	6.93	7.00	7.03
C1	-	5.25	-
D	0.30	0.35	0.40
E	1.00	1.04	1.10
E1	-	0.79	-
E2	-	0.25	-
Y	-	-	0.08

NOTES:

1. Bump counts : 36(8row x 6column)
2. Bump pitch : (x,y)=(0.75x0.75) (typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)

Package Dimension

48 pin FpBGA 6 x 7mm



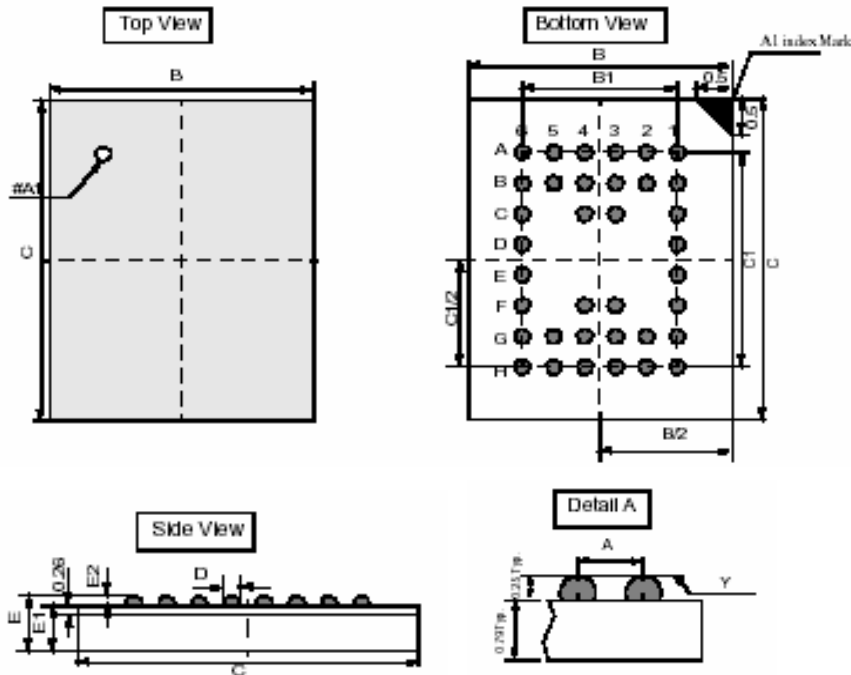
	Min	Typ	Max
A	-	0.75	-
B	5.93	6.00	6.03
B1	-	3.75	-
C	6.93	7.00	7.03
C1	-	5.25	-
D	0.30	0.35	0.40
E	1.00	1.04	1.10
E1	-	0.79	-
E2	-	0.25	-
Y	-	-	0.08

NOTES.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75x0.75) (typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)

Package Dimension

36 pin FpBGA 8 x 10mm



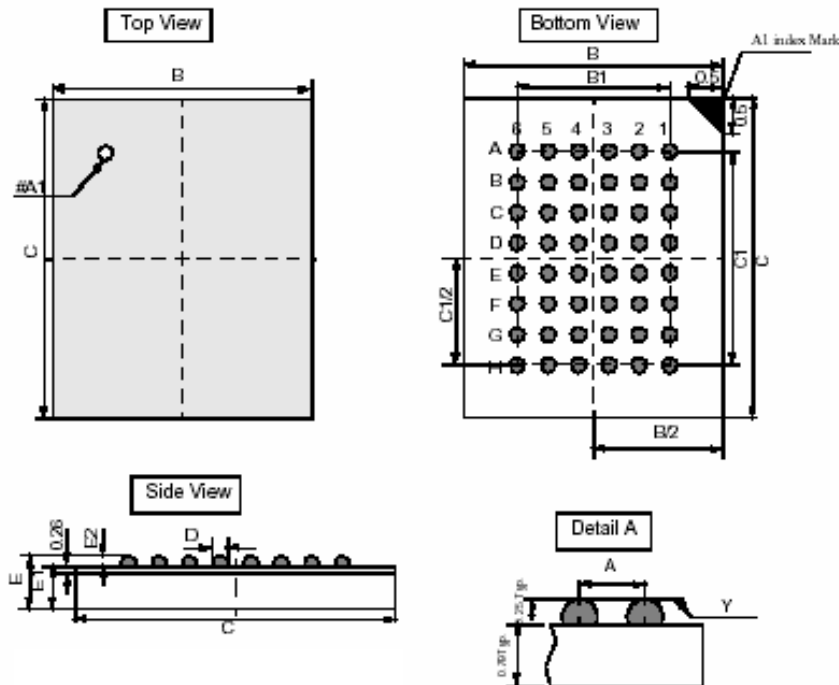
	Min	Typ	Max
A	-	0.75	-
B	7.90	8.00	8.10
B1	-	3.75	-
C	9.90	10.00	10.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	1.00	1.04	1.10
E1	-	0.79	-
E2	-	0.25	-
Y	-	-	0.08

NOTES.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75x0.75) (typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)

Package Dimension

48 pin FpBGA 8 x 10mm



	Min	Typ	Max
A	-	0.75	-
B	7.90	8.00	8.10
B1	-	3.75	-
C	9.90	10.00	10.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	1.00	1.04	1.10
E1	-	0.79	-
E2	-	0.25	-
Y	-	-	0.08

NOTES.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75x0.75) (typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)

Pin Configuration

1M SRAM(X8) 36 pin FpBGA

	1	2	3	4	5	6
A	A ₀	A ₁	CS ₂	A ₃	A ₆	A ₈
B	I/O ₅	A ₂	WE	A ₄	A ₇	I/O ₁
C	I/O ₆		DNU	A ₅		I/O ₂
D	V _{SS}					V _{CC}
E	V _{CC}					V _{SS}
F	I/O ₇		DNU	DNU		I/O ₃
G	I/O ₈	OE	CS ₁	A ₁₆	A ₁₅	I/O ₄
H	A ₉	A ₁₀	A ₁₁	A ₁₂	A ₁₃	A ₁₄

36-FPBGA : Top view (ball down)

Name	Function	Name	Function
CS ₁ ,CS ₂	Chip select inputs	WE	Write Enable input
OE	Output Enable input	V _{CC}	Power Supply
A ₀ -A ₁₆	Address Inputs	V _{SS}	Ground
I/O ₁ -I/O ₈	Data Inputs/outputs	DNU	Do Not Use

1M SRAM(X16) 48 pin FpBGA

(Dual CS)

	1	2	3	4	5	6
A	LB	OE	A ₀	A ₁	A ₂	CS ₂
B	I/O ₉	UB	A ₃	A ₄	CS ₁	I/O ₁
C	I/O ₁₀	I/O ₁₁	A ₅	A ₆	I/O ₂	I/O ₃
D	V _{SS}	I/O ₁₂	DNU	A ₇	I/O ₄	V _{CC}
E	V _{CC}	I/O ₁₃	DNU	DNU	I/O ₅	V _{SS}
F	I/O ₁₅	I/O ₁₄	A ₁₄	A ₁₅	I/O ₆	I/O ₇
G	I/O ₁₆	DNU	A ₁₂	A ₁₃	WE	I/O ₈
H	DNU	A ₈	A ₉	A ₁₀	A ₁₁	DNU

48-FPBGA : Top view (ball down)

Name	Function	Name	Function
CS ₁ ,CS ₂	Chip select inputs	V _{CC}	Power Supply
OE	Output Enable input	V _{SS}	Ground
WE	Write Enable input	UB	Upper Byte (I/O ₉₋₁₆)
A ₀ -A ₁₅	Address Inputs	LB	Lower Byte (I/O ₁₋₈)
I/O ₁ -I/O ₁₆	Data Inputs/outputs	DNU	Do Not Use

1M SRAM(X16) 48 pin FpBGA

(Single CS)

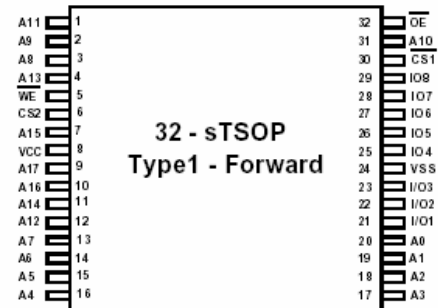
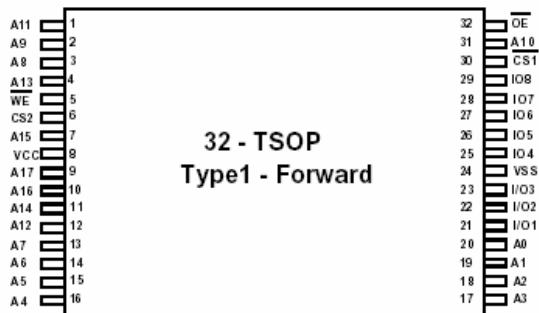
	1	2	3	4	5	6
A	LB	OE	A ₀	A ₁	A ₂	DNU
B	I/O ₉	UB	A ₃	A ₄	CS	I/O ₁
C	I/O ₁₀	I/O ₁₁	A ₅	A ₆	I/O ₂	I/O ₃
D	V _{SS}	I/O ₁₂	DNU	A ₇	I/O ₄	V _{CC}
E	V _{CC}	I/O ₁₃	DNU	DNU	I/O ₅	V _{SS}
F	I/O ₁₅	I/O ₁₄	A ₁₄	A ₁₅	I/O ₆	I/O ₇
G	I/O ₁₆	DNU	A ₁₂	A ₁₃	WE	I/O ₈
H	DNU	A ₈	A ₉	A ₁₀	A ₁₁	DNU

48-FPBGA : Top view (ball down)

Name	Function	Name	Function
CS	Chip select input	V _{CC}	Power Supply
OE	Output Enable input	V _{SS}	Ground
WE	Write Enable input	UB	Upper Byte (I/O ₉₋₁₆)
A ₀ -A ₁₅	Address Inputs	LB	Lower Byte (I/O ₁₋₈)
I/O ₁ -I/O ₁₆	Data Inputs/outputs	DNU	Do Not Use

Pin Configuration

2M SRAM (X8) 32 pin TSOP/sTSOP type I



Name	Function	Name	Function
$\overline{CS}_1, \overline{CS}_2$	Chip select inputs	\overline{WE}	Write Enable input
\overline{OE}	Output Enable input	Vcc	Power Supply
A ₀ ~A ₁₇	Address Inputs	Vss	Ground
I/O ₁ ~I/O ₈	Data Inputs/outputs	NC	No Connection

Name	Function	Name	Function
$\overline{CS}_1, \overline{CS}_2$	Chip select inputs	\overline{WE}	Write Enable input
\overline{OE}	Output Enable input	Vcc	Power Supply
A ₀ ~A ₁₇	Address Inputs	Vss	Ground
I/O ₁ ~I/O ₈	Data Inputs/outputs	NC	No Connection

Pin Configuration

2M SRAM(X8) 36 pin FpBGA

	1	2	3	4	5	6
A	A ₀	A ₁	CS ₂	A ₃	A ₆	A ₈
B	I/O ₅	A ₂	$\overline{\text{WE}}$	A ₄	A ₇	I/O ₁
C	I/O ₆		DNU	A ₅		I/O ₂
D	V _{SS}					V _{CC}
E	V _{CC}					V _{SS}
F	I/O ₇		DNU	A ₁₇		I/O ₃
G	I/O ₈	$\overline{\text{OE}}$	$\overline{\text{CS}}_1$	A ₁₆	A ₁₅	I/O ₄
H	A ₉	A ₁₀	A ₁₁	A ₁₂	A ₁₃	A ₁₄

36-FPBGA : Top view (ball down)

Name	Function	Name	Function
$\overline{\text{CS}}_1, \text{CS}_2$	Chip select inputs	$\overline{\text{WE}}$	Write Enable input
$\overline{\text{OE}}$	Output Enable input	V _{CC}	Power Supply
A ₀ -A ₁₇	Address Inputs	V _{SS}	Ground
I/O ₁ -I/O ₈	Data Inputs/outputs	DNU	Do Not Use

2M SRAM(X16) 48 pin FpBGA
(Dual CS)

	1	2	3	4	5	6
A	$\overline{\text{LB}}$	$\overline{\text{OE}}$	A ₀	A ₁	A ₂	CS ₂
B	I/O ₉	$\overline{\text{UB}}$	A ₃	A ₄	$\overline{\text{CS}}_1$	I/O ₁
C	I/O ₁₀	I/O ₁₁	A ₅	A ₆	I/O ₂	I/O ₃
D	V _{SS}	I/O ₁₂	DNU	A ₇	I/O ₄	V _{CC}
E	V _{CC}	I/O ₁₃	DNU	A ₁₆	I/O ₅	V _{SS}
F	I/O ₁₅	I/O ₁₄	A ₁₄	A ₁₅	I/O ₆	I/O ₇
G	I/O ₁₆	DNU	A ₁₂	A ₁₃	$\overline{\text{WE}}$	I/O ₈
H	DNU	A ₈	A ₉	A ₁₀	A ₁₁	DNU

48-FPBGA : Top view (ball down)

Name	Function	Name	Function
$\overline{\text{CS}}_1, \text{CS}_2$	Chip select inputs	V _{CC}	Power Supply
$\overline{\text{OE}}$	Output Enable input	V _{SS}	Ground
$\overline{\text{WE}}$	Write Enable input	$\overline{\text{UB}}$	Upper Byte (I/O ₉₋₁₆)
A ₀ -A ₁₆	Address Inputs	$\overline{\text{LB}}$	Lower Byte (I/O ₁₋₈)
I/O ₁ -I/O ₁₆	Data Inputs/outputs	DNU	Do Not Use

2M SRAM(X16) 48 pin FpBGA
(Single CS)

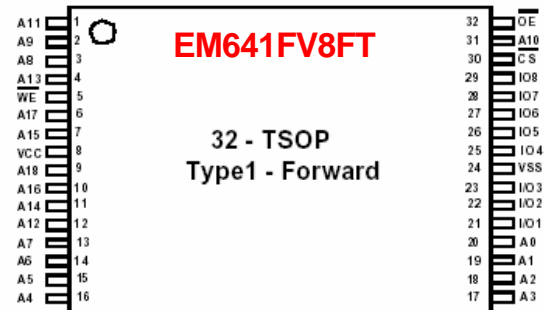
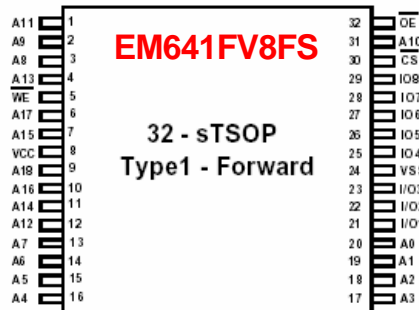
	1	2	3	4	5	6
A	$\overline{\text{LB}}$	$\overline{\text{OE}}$	A ₀	A ₁	A ₂	DNU
B	I/O ₉	$\overline{\text{UB}}$	A ₃	A ₄	$\overline{\text{CS}}$	I/O ₁
C	I/O ₁₀	I/O ₁₁	A ₅	A ₆	I/O ₂	I/O ₃
D	V _{SS}	I/O ₁₂	DNU	A ₇	I/O ₄	V _{CC}
E	V _{CC}	I/O ₁₃	DNU	A ₁₆	I/O ₅	V _{SS}
F	I/O ₁₅	I/O ₁₄	A ₁₄	A ₁₅	I/O ₆	I/O ₇
G	I/O ₁₆	DNU	A ₁₂	A ₁₃	$\overline{\text{WE}}$	I/O ₈
H	DNU	A ₈	A ₉	A ₁₀	A ₁₁	DNU

48-FPBGA : Top view (ball down)

Name	Function	Name	Function
$\overline{\text{CS}}$	Chip select input	V _{CC}	Power Supply
$\overline{\text{OE}}$	Output Enable input	V _{SS}	Ground
$\overline{\text{WE}}$	Write Enable input	$\overline{\text{UB}}$	Upper Byte (I/O ₉₋₁₆)
A ₀ -A ₁₆	Address Inputs	$\overline{\text{LB}}$	Lower Byte (I/O ₁₋₈)
I/O ₁ -I/O ₁₆	Data Inputs/outputs	DNU	Do Not Use

Pin Configuration

4M SRAM(X8) 32 pin TSOP/sTSOP type I

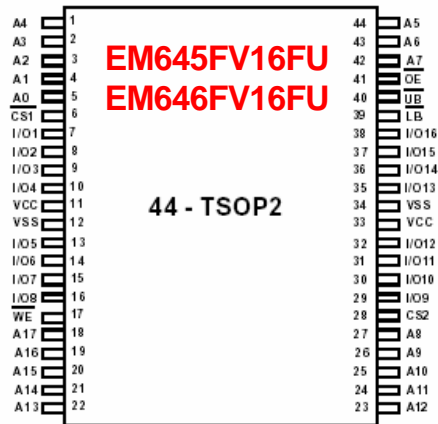


Name	Function	Name	Function
\overline{CS}	Chip select inputs	\overline{WE}	Write Enable input
\overline{OE}	Output Enable input	Vcc	Power Supply
A ₀ ~A ₁₈	Address Inputs	Vss	Ground
I/O ₁ ~I/O ₈	Data Inputs/outputs	NC	No Connection

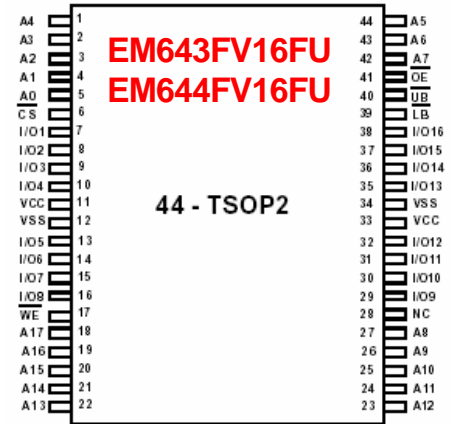
Name	Function	Name	Function
\overline{CS}	Chip select inputs	\overline{WE}	Write Enable input
\overline{OE}	Output Enable input	Vcc	Power Supply
A ₀ ~A ₁₈	Address Inputs	Vss	Ground
I/O ₁ ~I/O ₈	Data Inputs/outputs	NC	No Connection

Pin Configuration

4M SRAM(X16) 44 pin TSOP type II



Name	Function	Name	Function
$\overline{CS}_1, \overline{CS}_2$	Chip select inputs	Vcc	Power Supply
\overline{OE}	Output Enable input	Vss	Ground
\overline{WE}	Write Enable input	\overline{UB}	Upper Byte (I/O ₉₋₁₆)
A ₀ ~A ₁₇	Address Inputs	\overline{LB}	Lower Byte (I/O ₁₋₈)
I/O ₁ ~I/O ₁₆	Data Inputs/outputs	NC	No Connection



Name	Function	Name	Function
\overline{CS}	Chip select input	Vcc	Power Supply
\overline{OE}	Output Enable input	Vss	Ground
\overline{WE}	Write Enable input	\overline{UB}	Upper Byte (I/O ₉₋₁₆)
A ₀ ~A ₁₇	Address Inputs	\overline{LB}	Lower Byte (I/O ₁₋₈)
I/O ₁ ~I/O ₁₆	Data Inputs/outputs	NC	No Connection

Pin Configuration

4M SRAM(X8) 36 pin FpBGA

	1	2	3	4	5	6
A	A ₀	A ₁	CS ₂	A ₃	A ₆	A ₈
B	I/O ₅	A ₂	WE	A ₄	A ₇	I/O ₁
C	I/O ₆		DNU	A ₅		I/O ₂
D	V _{SS}					V _{CC}
E	V _{CC}					V _{SS}
F	I/O ₇		A ₁₈	A ₁₇		I/O ₃
G	I/O ₈	OE	CS ₁	A ₁₆	A ₁₅	I/O ₄
H	A ₉	A ₁₀	A ₁₁	A ₁₂	A ₁₃	A ₁₄

36-FPBGA : Top view (ball down)

Name	Function	Name	Function
CS ₁ , CS ₂	Chip select inputs	WE	Write Enable input
OE	Output Enable input	V _{CC}	Power Supply
A ₀ ~A ₁₈	Address Inputs	V _{SS}	Ground
I/O ₁ ~I/O ₈	Data Inputs/outputs	DNU	Do Not Use

4M SRAM(X16) 48 pin FpBGA

(Dual CS)

	1	2	3	4	5	6
A	LB	OE	A ₀	A ₁	A ₂	CS ₂
B	I/O ₉	UB	A ₃	A ₄	CS ₁	I/O ₁
C	I/O ₁₀	I/O ₁₁	A ₅	A ₆	I/O ₂	I/O ₃
D	V _{SS}	I/O ₁₂	A ₁₇	A ₇	I/O ₄	V _{CC}
E	V _{CC}	I/O ₁₃	DNU	A ₁₆	I/O ₅	V _{SS}
F	I/O ₁₅	I/O ₁₄	A ₁₄	A ₁₅	I/O ₆	I/O ₇
G	I/O ₁₆	DNU	A ₁₂	A ₁₃	WE	I/O ₈
H	DNU	A ₈	A ₉	A ₁₀	A ₁₁	DNU

48-FPBGA : Top view (ball down)

Name	Function	Name	Function
CS ₁ , CS ₂	Chip select inputs	V _{CC}	Power Supply
OE	Output Enable input	V _{SS}	Ground
WE	Write Enable input	UB	Upper Byte (I/O ₉₋₁₆)
A ₀ ~A ₁₇	Address Inputs	LB	Lower Byte (I/O ₁₋₈)
I/O ₁ ~I/O ₁₆	Data Inputs/outputs	DNU	Do Not Use

4M SRAM(X16) 48 pin FpBGA

(Single CS)

	1	2	3	4	5	6
A	LB	OE	A ₀	A ₁	A ₂	DNU
B	I/O ₉	UB	A ₃	A ₄	CS	I/O ₁
C	I/O ₁₀	I/O ₁₁	A ₅	A ₆	I/O ₂	I/O ₃
D	V _{SS}	I/O ₁₂	A ₁₇	A ₇	I/O ₄	V _{CC}
E	V _{CC}	I/O ₁₃	DNU	A ₁₆	I/O ₅	V _{SS}
F	I/O ₁₅	I/O ₁₄	A ₁₄	A ₁₅	I/O ₆	I/O ₇
G	I/O ₁₆	DNU	A ₁₂	A ₁₃	WE	I/O ₈
H	DNU	A ₈	A ₉	A ₁₀	A ₁₁	DNU

48-FPBGA : Top view (ball down)

Name	Function	Name	Function
CS	Chip select input	V _{CC}	Power Supply
OE	Output Enable input	V _{SS}	Ground
WE	Write Enable input	UB	Upper Byte (I/O ₉₋₁₆)
A ₀ ~A ₁₇	Address Inputs	LB	Lower Byte (I/O ₁₋₈)
I/O ₁ ~I/O ₁₆	Data Inputs/outputs	DNU	Do Not Use

Pin Configuration

8M SRAM(X8) 36 pin FpBGA

	1	2	3	4	5	6
A	A ₀	A ₁	CS ₂	A ₃	A ₆	A ₈
B	I/O ₅	A ₂	WE	A ₄	A ₇	I/O ₁
C	I/O ₆		A ₁₉	A ₅		I/O ₂
D	V _{SS}					V _{CC}
E	V _{CC}					V _{SS}
F	I/O ₇		A ₁₈	A ₁₇		I/O ₃
G	I/O ₈	OE	CS ₁	A ₁₆	A ₁₅	I/O ₄
H	A ₉	A ₁₀	A ₁₁	A ₁₂	A ₁₃	A ₁₄

36-FPBG : Top view (ball down)

Name	Function	Name	Function
CS ₁ ,CS ₂	Chip select inputs	WE	Write Enable input
OE	Output Enable input	V _{CC}	Power Supply
A ₀ ~A ₁₉	Address Inputs	V _{SS}	Ground
I/O ₁ ~I/O ₈	Data Inputs/outputs		

8M SRAM(X16) 48 pin FpBGA

(Dual CS)

	1	2	3	4	5	6
A	LB	OE	A ₀	A ₁	A ₂	CS ₂
B	I/O ₉	UB	A ₃	A ₄	CS ₁	I/O ₁
C	I/O ₁₀	I/O ₁₁	A ₅	A ₆	I/O ₂	I/O ₃
D	V _{SS}	I/O ₁₂	A ₁₇	A ₇	I/O ₄	V _{CC}
E	V _{CC}	I/O ₁₃	DNU	A ₁₆	I/O ₅	V _{SS}
F	I/O ₁₅	I/O ₁₄	A ₁₄	A ₁₅	I/O ₆	I/O ₇
G	I/O ₁₆	DNU	A ₁₂	A ₁₃	WE	I/O ₈
H	A ₁₈	A ₈	A ₉	A ₁₀	A ₁₁	DNU

48-FPBG : Top view (ball down)

Name	Function	Name	Function
CS ₁ ,CS ₂	Chip select inputs	V _{CC}	Power Supply
OE	Output Enable input	V _{SS}	Ground
WE	Write Enable input	UB	Upper Byte (I/O ₉₋₁₆)
A ₀ ~A ₁₈	Address Inputs	LB	Lower Byte (I/O ₁₋₈)
I/O ₁ ~I/O ₁₆	Data Inputs/outputs	DNU	Do Not Use

8M SRAM(X16) 48 pin FpBGA

(Single CS)

	1	2	3	4	5	6
A	LB	OE	A ₀	A ₁	A ₂	DNU
B	I/O ₉	UB	A ₃	A ₄	CS	I/O ₁
C	I/O ₁₀	I/O ₁₁	A ₅	A ₆	I/O ₂	I/O ₃
D	V _{SS}	I/O ₁₂	A ₁₇	A ₇	I/O ₄	V _{CC}
E	V _{CC}	I/O ₁₃	DNU	A ₁₆	I/O ₅	V _{SS}
F	I/O ₁₅	I/O ₁₄	A ₁₄	A ₁₅	I/O ₆	I/O ₇
G	I/O ₁₆	DNU	A ₁₂	A ₁₃	WE	I/O ₈
H	A ₁₈	A ₈	A ₉	A ₁₀	A ₁₁	DNU

48-FPBG : Top view (ball down)

Name	Function	Name	Function
CS	Chip select input	V _{CC}	Power Supply
OE	Output Enable input	V _{SS}	Ground
WE	Write Enable input	UB	Upper Byte (I/O ₉₋₁₆)
A ₀ ~A ₁₈	Address Inputs	LB	Lower Byte (I/O ₁₋₈)
I/O ₁ ~I/O ₁₆	Data Inputs/outputs	DNU	Do Not Use